WHAT IS CLAIMED IS:

1. A method for fabricating a shallow trench isolation region, comprising:

blanket depositing a trench fill material over a semiconductor topography comprising one or more trenches;

polishing said semiconductor topography to form an upper surface of the semiconductor topography at an elevation above the trenches, wherein the upper surface does not comprise a polish stop material; and

etching an entirety of the upper surface simultaneously, wherein remaining portions of the trench fill material are laterally confined within the trenches.

2. The method of claim 1, wherein an upper surface of the remaining portions is above an upper surface of a semiconductor substrate within the semiconductor topography.

3. The method of claim 2, wherein said upper surface of the remaining portions is less than approximately 200 angstroms above the upper surface of the semiconductor substrate.

4. The method of claim 1, wherein said polishing comprises a fixed abrasive polishing process.

5. The method of claim 1, further comprising forming an intermediate layer upon an upper surface of the semiconductor topography prior to said depositing trench fill material, and wherein said etching comprises etching at least a portion of the intermediate layer.

6. The method of claim 5, wherein said intermediate layer comprises a base oxide layer.

7. The method of claim 5, wherein said intermediate layer further comprises a doped oxide layer.

8. The method of claim 7, wherein said doped oxide layer comprises borophosphosilicate glass.

9. The method of claim 5, wherein said intermediate layer further comprises a nitride layer, and wherein a thickness of said nitride layer is less than approximately 500 angstroms.

10. The method of claim 5, wherein said intermediate layer further comprises a silicon carbide layer.

11. The method of claim 5, wherein said intermediate layer further comprises a carbonated polymer layer.

12. A method for processing a semiconductor topography, comprising:

polishing an upper layer of said semiconductor topography to form an upper surface of the semiconductor topography at an elevation above an underlying layer, wherein said underlying layer comprises a lateral variation in polishing characteristics; and

etching the entirety of the upper surface of the semiconductor topography simultaneously to expose the underlying layer.

13. The method of claim 12, wherein said upper surface of the semiconductor topography is spaced sufficiently above the underlying layer to avoid dishing during said polishing.

14. The method of claim 12, wherein said upper surface of the semiconductor topography is spaced sufficiently above the underlying layer to avoid polishing the underlying layer.

15. The method of claim 12, wherein said elevation is between approximately 100 angstroms and approximately 1000 angstroms.

16. The method of claim 12, wherein said polishing comprises a fixed abrasive polishing process.

17. The method of claim 12, wherein said upper layer comprises an interlevel dielectric layer.

18. The method of claim 17, wherein said interlevel dielectric layer comprises silicon dioxide.

19. The method of claim 12, wherein said underlying layer comprises a silicon substrate patterned with dielectric filled trenches.

20. The method of claim 12, wherein said underlying layer comprises silicon nitride regions laterally interspersed with silicon dioxide regions.

21. The method of claim 12, wherein said underlying layer comprises conductive regions interspersed with dielectric regions.

22. A method for processing a semiconductor topography, comprising using fixed abrasive polishing of a dielectric layer for reducing a required thickness of an additional layer underlying the dielectric layer.

23. The method of claim 22, wherein said additional layer has different polishing characteristics than the dielectric layer.

24. The method of claim 22, wherein said reducing comprises forming the additional layer with a thickness of less than approximately 500 angstroms.

25. The method of claim 22, wherein said reducing comprises forming the additional layer with a thickness of approximately 150 angstroms or less.

26. The method of claim 22, wherein said reducing comprises eliminating the additional layer.

27. The method of claim 22, wherein the dielectric layer comprises a trench fill layer for shallow trench isolation regions.

28. The method of claim 22, wherein the dielectric layer comprises an interlevel dielectric layer.

29. The method of claim 22, wherein said fixed abrasive polishing process comprises applying a fluid substantially free of particulate matter between the semiconductor topography and an abrasive polishing surface.

30. The method of claim 22, further comprising etching the dielectric layer subsequent to said fixed abrasive polishing the dielectric layer.